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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/493,319	01/28/2000	Samson Huang	INTL-0312-US (P7995)	2102

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EXAMINER	
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ART UNIT	PAPER NUMBER
2675	16

DATE MAILED: 12/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/493,319	HUANG, SAMSON	
	Examiner	Art Unit	
	Leland R. Jorgensen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *45 - 54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *45 - 54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 45 – 48 and 50 - 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima, USPN 6,333,737 B1, in view of Nishida, USPN 6,297,787 B1.

Claims 45 and 50

Nakajima teaches a pixel 2 for a liquid crystal display. Nakajima, figures 1 and 2; col. 2, lines 44 – 47; and col. 3, lines 11 – 17. Nakajima teaches a memory 22 for each pixel. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1a. Nakajima teaches a digital to analog conversion circuit 25. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1. Although Nakajima does not specifically describe converting the digital indication into an analog voltage during a refresh operation, it is inherent to the operation of such a circuit that the information would be changed during a refresh operation. See Nakajima, col. 1, lines 13 – 19.

Nakajima does not teach that each memory is associated with a group of two or more of the pixel cells and that the memory is located closer to the associated group of pixel cells than another one of the group of pixel cells.

Nishida teaches an array of pixel cells having a memory 332 for each display element 333. Nishida, col. 6, lines 16 – 18; col. 12, lines 9 – 26; and figure 12. Nishida teaches that the memory cells are changed during a refresh operation. Nishida, col. 9, lines 10 – 45; col. 10, lines 18 – 43. Nishida teaches that each single display unit [display unit 80] can include a

plurality of pixels [unit case 85]. Each pixel [unit case 85 consists of three light emitting diodes [83R, 83G, and 83B]. Nishida, col. 13, lines 43 – 60; and figure 10. Nishida, after giving an example of a display unit having sixteen sets of pixels with three lights each, states, "In such a configuration, it is still sufficient to provide single memory and single controller for the single display unit, since display information with respect to respective forty-eight light emitting diodes can be stored into the single memory." Nishida, col. 13, lines 56 – 60.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide memory to multiple pixels as taught by Nishida with the light modulator array as taught by Nakajima. Such combination would reduce components and costs without decreasing the advantages of the invention of Nakajima.

Claims 46

Nakajima teaches that the memory 22 is local to the pixel cell. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1a. Nishida teaches that the memory is local to the pixel group. Nishida, col. 13, lines 43 – 60; and figure 12.

Claims 47 and 52

Nakajima teaches that the memory may be a RAM. Nakajima, col. 3, lines 57 – 59. Nishida teaches that the memory may be RAM. Nishida, col. 13, lines 21 – 26.

Claim 48

Nakajima teaches reading the digital indication from the memory. Nakajima, col. 3, line 66 – col. 4, line 4; and col. 5, lines 51 – 52. Nakajima does not specifically describe the reading during the refresh operation, but it is inherent to the operation of such a circuit that the information would be changed during a refresh operation. See Nakajima, col. 1, lines 13 – 19.

Claim 51

It is inherent to the operation of Nakajima that the refresh operation occurs at a different rate than the frame update operation. Nakajima specifically teaches,

> Further, if each pixel is provided with the output means for outputting data for displaying pixels (display data) on the basis of the processed data in addition to the operating means, the operational processing can be immediately performed on the data input to a pixel from the external or adjacent pixels to display the pixel concerned.

Nakajima, col. 2, lines 14 – 20. See also: Nakajima, col. 5, lines 17 – 26; col. 5, line 42 – col. 6, line 3.

Claims 53 and 54

It is inherent to Nakajima that each of the pixel cells is controlled independently with respect to the other pixel cells. Nakajima, col. 1, lines 50 – 65. The single memory in Nishida retains display information about each of the pixel cells in each group of pixel cells. Nishida, col. 13, lines 52 – 60.

3. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima in view of Nishida as applied to claim 45 above, and further in view of Kinoshita et al, USPN 5,771,031.

Claims 49

As understood in the art, latching is holding data in a circuit until other circuits are ready to change the latch circuit. Nakajima does not specifically teach the step of latching the information from the memory.

Kinoshita teaches the step of latching the information from the memory while the data is updated. Kinoshita, col. 6, lines 39 – 42; col. 6, lines 63 – col. 7, line 6; col. 7, lines 14 – 21, lines 46 – 67; and col. 9, line 59 – col. 10, line 67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the latching method and circuit taught by Kinoshita the method as taught by Nakajima and Nishida. Like Nakajima, Kinoshita teaches a drive method for individual pixels of a flat panel display. Kinoshita, col. 1, lines 5 –8; and col. 3, lines 60 –65. Both Nakajima and Kinoshita teach many of the same parts including storage capacitors, CS, memory, and digital to analog converters. See e.g. Kinoshita, figures 1, 3 & 4; col. 4, lines 33 –36; col. 5, lines 64 – 66; col. 7, lines 14 – 21; and col. 8, lines 11 – 14. Both teach the need to individually drive each pixel array. Kinoshita, col. 1, line 10 – col. 2, line 37; and col. 2, lines 6 – 9. Kinoshita invites such combination by teaching,

> In the trend of resent years, the number of pixels in each horizontal pixel array is increased to improve the resolution of the active matrix LCD, and the word length of each pixel data is also increased to improve the precision of the gray scale. In order to increase the number of pixels and the word length, it is necessary for the signal line driving circuit to process the pixel data at a higher speed. However, if the processing speed of the signal line driving circuit is improved to its limit, it is difficult to drive all the signal lines within one horizontal scanning period.

Kinoshita, col. 1, lines 28 – 37. Kinoshita adds as the object of invention,

> An object of the present invention is to provide a flat-panel display device and a method of driving the same, which can maintain the memory capacity required for block-driving of each horizontal pixel array to be small.

Kinoshita, col. 2, lines 6 – 9. Kinoshita further adds,

> According to the aforementioned flat-panel display device and its driving method, pixel data items sequentially supplied from outside are divided into pixel-data blocks each consisting of the same number of pixel data items, equivalent to

> the number of pixels forming one pixel block. M pixel-data blocks are sequentially written in M memory sections, and the M pixel-data blocks stored in the M memory sections are read in parallel while writing is performed. These M pixel-data blocks are supplied to corresponding ones of the data supply buses. Therefore, the total memory capacity of the memory sections is smaller than a memory capacity required for storing all items of pixel data for one horizontal pixel array. Further, the memory capacity of the memory section is not significantly depend on the number of pixel data items for one horizontal array and the word length of pixel data. This enables an increase in the number of pixel data items for one horizontal pixel array and an increase in the word length while maintaining the memory capacity of the memory section to be small. As a result of this, it is possible to prevent costs for manufacturing a flat-panel display device from being increased due to block driving of the horizontal pixel array.

Kinoshita, col. 2, line 63 – col. 3, line 17. Kinoshita teaches that the memory can be reduced with its latching circuit. Kinoshita, col. 9, lines 59 – 67; and col. 10, lines 60 – 67.

Response to Arguments

4. Applicant's arguments filed 27 October 2003 have been fully considered but they are not persuasive.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine a memory to multiple pixels as taught by Nishida with the light modulator array as taught by Nakajima, to reduce the costs and complexity needed to provide a separate

memory at each single pixel while still providing the advantages of the invention of Nakajima. Both Nakajima and Nishida invite such combination. Nakajima suggests that one in the art could consider a number of different combinations. Nakajima teaches,

> In this embodiment, all of the operating means, the output means, the storage means and the input means are provided to each pixel. However, the present invention is not limited to the above mode. That is, there may be provided a liquid crystal display device in which only the operating means, the combination of the operating means and the output means, the combination of the operating means, the output means and the storage means or any combination of the above means may be selected and provided to each pixel in association with the function added to the liquid crystal display device. Of course, the above combination may be applied to other display devices.
>
> Further, any combination of the input circuit and the final output circuit (for example, only the input circuit, the combination of the input circuit and the final output circuit, and the final output circuit) or any combination of the first controller, the second controller and the third controller in place of any combination of the input circuit and the final output circuit may be used in association with the combination of the above means. Besides, any combination of the input circuit, the final output circuit, the first controller, the second controller and the third controller may be used in association with the combination of the above means. That is, the various modifications may be made in association with the functions to be added to the liquid crystal display device.

Nakajima, col. 6, line 53 – col. 7, line 11. Nishida also teaches the advantages of a memory for each pixel but then teaches the advantages of providing a memory for a group of pixels. Nishida teaches,

> In this case, sixteen sets of pixel component each comprised of three light emitting diodes are provided within the single display unit so that forty-eight light emitting diodes in total and forty-eight regulators in total are included there within. In such a configuration, it is still sufficient to provide single memory and single controller for the single display unit, since display information with respect to respective forty-eight light emitting diodes can be stored into the single memory.

Nishida, col. 13, lines 52 – 60. Thus, Nishida suggests that a single memory for a group of pixels can store individual information for each pixel.

Applicant also argued that Nishida does not teach that each memory is associated with a group of two or more of the pixel cells. Nishida, however, teaches a memory for each display unit 80. In figure 10, Nishida shows that a display unit can include sixteen unit cases 85 or sets of pixel components. See Nishida, col. 13, lines 52 – 60 cited above in the prior paragraph. Each unit case 85 or pixel component consists of three light emitting diodes [83R, 83G, and 83B]. Nishida, col. 13, lines 43 – 60; and figure 10. Applicant's argument suggests that whole display unit is a pixel. This is incorrect. As understood in the art, a pixel is defined as follows,

> **Pixel** n. Short for picture (**pix**) **el**ement. One spot in a rectilinear grid of thousands of such spots that are individually "painted" to form an image produced on the screen by a computer or on paper by a printer. A pixel is the smallest element that display or print hardware and software can manipulate in creating letters, numbers, or graphics.

Microsoft Computer Dictionary, 4th Ed. (1999), p. 345. In the art, generally a color pixel consists of the three primary colors, each designated a subpixel. Thus, the smallest element on Nishida is the unit case 85 (or pixel component). The memory described in Nishida, col. 13, lines 52 – 60 supports forty-eight light emitting diodes, broken up into sixteen pixels each composed of three subpixels [83R, 83G, and 83B].

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland Jorgensen whose telephone number is 703-305-2650. The examiner can normally be reached on Monday through Friday, 7:00 a.m. through 3:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on 703-305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, telephone number (703) 306-0377.

lrj

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600